Amendments to the Drawings:

The attached replacement sheets of drawings include changes to Fig. 1. The replacement sheet including Fig. 1 replaces the original sheet including Fig. 1.

Attachment: Replacement Sheet 1 page

REMARKS/ARGUMENTS

1. Amendments to the Drawings

Fig. 1 is revised to include a previously omitted reference sign mentioned in paragraph 29 of the specification being loop count register 66. No new matter is introduced.

Consideration of the amendment to the drawing is respectfully requested.

2. Amendments to the Claims

Claim 3 is currently amended to replace "the third memory" with "the first memory" as recited in claim 2 in response to Examiner's objection of insufficient antecedent basis for the limitation in the claim. No new matter is introduced. Consideration of amended claim 3 is respectfully requested.

Claim 4 is currently amended to replace "the third memory" with "the first memory" as recited in claim 2 in response to Examiner's objection of insufficient antecedent basis for the limitation in the claim. No new matter is introduced. Consideration of amended claim 4 is respectfully requested.

Claim 10 is currently amended to replace "the first memory" with "the third memory" as recited in claim 9 in response to Examiner's objection of insufficient antecedent basis for the limitation in the claim. No new matter is introduced. Consideration of amended claim 10 is respectfully requested.

Claims 12-14 are newly entered based on original claims 1, 2, 9 and specification paragraph [0037]. No new matter is introduced. Consideration of new claims 12-14 is respectfully requested.

3. Claim Objections

Claims 3, 4, and 10 are objected to because there is insufficient antecedent basis for the limitations in the claims. The assumptions made by Examiner were all correct and claims 3, 4, and 10 are currently amended to correspond to Examiner's assumptions that are fully supported in the specification. Applicant believes the objections are overcome now.

4. Claim Rejections

Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Catherwood et al. (U.S. Patent No. 6,976,158 B2).

Response:

Claim 1

Catherwood et al. teach methods for relieving the limitation of executing a target instruction a limited number of times due to limited storage capacity for a loop count value. Specifically, Catherwood et al. disclose in col. 8, lines 59 – 60, "...the processor stores a loop count value into a repeat count register." Although the utilization of the repeat count register provides for increased looping capacity, it does not offer any processor cycle savings or efficiency improvements because the REPEAT instruction has to be executed prior to the target instruction (col. 3, lines 58-60). The applicant provides a dedicated loop counter as well, and additionally the claimed invention proceeds to loop the preceding instruction, i.e., the instruction just prior to the loop instruction (see Step 170 in paragraph [0031]) and furthermore in paragraph [0040], "Using a loop process, the program would list instruction A first followed by a loop instruction...because instruction A is listed first, the processing unit will have already fetched instruction A before reaching the loop instruction. Consequently, when the processing unit executes the loop instruction in the second cycle, instruction A has already been fetched. As a result, the processing unit in the second cycle can execute both the loop instruction and instruction A." Therefore, the processing unit requires only 1 cycle for each execution of instruction A and for a total of, for example, X repetitions, X cycles are

needed. Regarding the prior art, and specifically, Catherwood et al, an instruction to be looped (i.e., repeated) X times requires X+1 processor cycles.

Applicant maintains that the claimed feature "the processing unit will loop the instruction previous to the loop instruction a number of times as defined by the loop count value" is not taught or suggested by Catherwood et al. Applicant further maintains that this feature of the claimed invention is not obvious for a person of ordinary skill in the art in view of the teachings of Catherwood et al. The rejection under 35 U.S.C. 102(e) is overcome accordingly. Applicant respectfully requests reconsideration of claim 1.

Claims 2-11

Claims 2 - 11 are dependent on claim 1 and should be allowable if claim 1 is found allowable. Reconsideration of claims 2 - 11 is respectfully requested.

New claims 12-14

Catherwood et al. do not teach, column 7, lines 20-24, a REPEAT W instruction where W stands for the W register and according to the REPEAT W instruction, the instruction specifies a W register by including its address within the instruction and that the specified W register stores the loop count value for the repeat loop. However, Catherwood et al. fail to teach as the applicant has disclosed in paragraph [0037], the claimed feature of the mechanism by which the claimed invention's loop count value, for example, the repeat loop, is obtained by decoding an instruction with an address of a table entry. Please note that, for example, the table can be stored in the set of address registers 52. Next, the table is accessed at said table entry based on the decoded instruction. At the said table entry, an address value is stored that indicates where in the RAM 54 the loop count value is stored.

Additionally, Catherwood et al. do not disclose the method of storing a table containing addresses of a plurality of loop count values, as is disclosed by applicant in paragraph [0022], "Prior to the beginning of the flowchart, a table of the address of a plurality of loop count values is loaded from the program stored in the ROM 20 into the address registers 52." Applicant believes these newly claimed features of the claimed invention are not obvious for a person of ordinary skill in the art in view of the teachings of Catherwood et al. Applicant respectfully requests consideration of newly entered claims 12-14.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 05/21/2006

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)